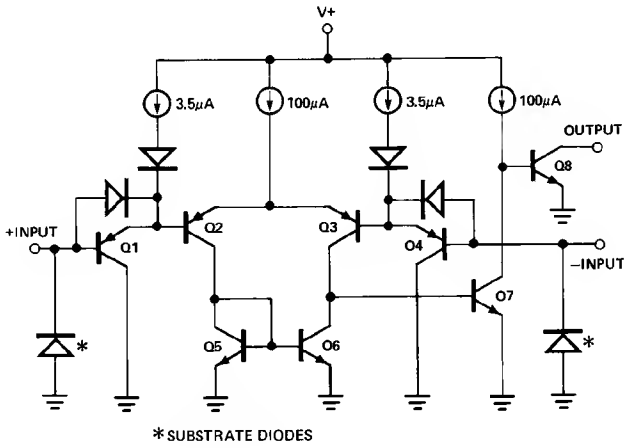
Quad Low Power, Precision Comparator

CMP04

FEATURES

- **High Gain: 200 V/mV typ**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5 mW/Comparator)**
- **Low Input Bias Current: 100 nA max**
- **Low Input Ottset Current: 10 nA max**
- **Low Offset Voltage: 1 mV max**
- **Low Output Saturation Voltage: 250 mV @ 4 mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**
- **Available in Die Form**

SIMPLIFIED SCHEMATIC (1/4 CMP-04)

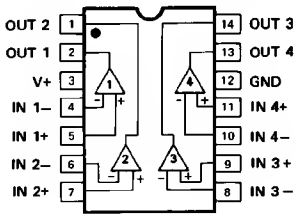


GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2 mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

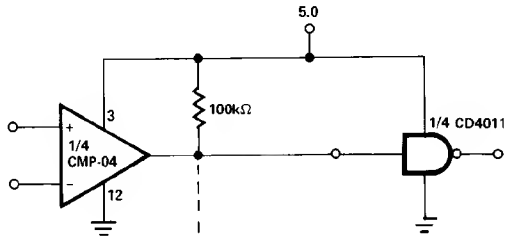
PIN CONNECTIONS

14-Pin Hermetic DIP (Y Suffix)
14-Pin Epoxy DIP (P Suffix)
14-Pin SO (S Suffix)

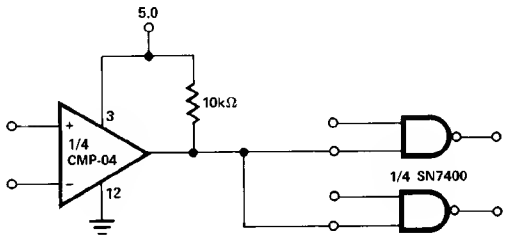


TYPICAL INTERFACE

Driving CMOS



Driving TTL



REV. B

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Tel: 617/329-4700 **Fax: 617/326-8703**

CMP04- SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V+ = +5 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 0 Ω, R_L = 5.1 kΩ, V_O = 1.4 V[1]		0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$, R_L = 5.1 kΩ V_O = 1.4 V		2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		25	100	nA
Voltage Gain	A_V	$R_L \geq 15$ kΩ, V+ = 15 V[5]	80	200		V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V[4] V_{RL} = 5 V, R_L = 5.1 kΩ		300		ns
Small-Signal Response Time	t_r	V_{IN} = 100 mV Step[4], 5 mV Overdrive V_{RL} = 5 V, R_L = 5.1 kΩ		1.3		µs
Input Voltage Range	CMVR	(Note 2)	0		V+ – 1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100		dB
Power Supply Rejection Ratio	PSRR	V+ = +5 V to +18 V[5]	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+)$ = 0, $I_{SINK} \leq 4$ mA		250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+)$ = 0, $V_O \leq 1.5$ V	6	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1$ V, $V_{IN}(-)$ = 0, V_O = 30 V		0.1	100	nA
Supply Current	I+	$R_L = \infty$, All Comps, V+ = 30 V		0.8	2.0	mA

NOTES
[1]At output switch point, V_O = 1.4 V, R_S = 0 Ω with V+ from 5 V; and over the full input common-mode range (0 V to V+ – 1.5 V).
[2]The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ – 1.5 V, but either or both inputs can go to +30 V without damage.
[3]$R_L \geq 15$ kΩ, V+ = 15 V, V_{CM} = 1.5 V to 13.5 V.
[4]Sample tested.
[5]Guaranteed by design.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 36 V or ±18 V
Differential Input Voltage . . . . . 36 Vdc
Input Voltage . . . . . –0.3 V to +36 V
Operating Temperature Range
  CMP04FY . . . . . –40°C to +85°C
  CMP04BY . . . . . –55°C to +125°C
  CMP04FP, FS . . . . . –40°C to +85°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
  (P Suffix) . . . . . –65°C to +125°C
Input Current (V_{IN} < –3.0 V) . . . . . 50 mA
Output Short-Circuit to GND . . . . . Continuous
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for Cerdip and Plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

Model	T_A = +25°C V_{OS}	Temperature Range	Package Descriptions	Package Options
CMP04BY/883C	1 mV	–55°C to +125°C	14-Contact LCC	Q-14
CMP04FP	1 mV	–40°C to +85°C	14-Pin P-DIP	N-14
CMP04FS	1 mV	–40°C to +85°C	14-Pin SO	SO-14

*Burn-in is available on commercial and industrial temperature range parts in Cerdip and plastic DIP packages.

ELECTRICAL CHARACTERISTICS

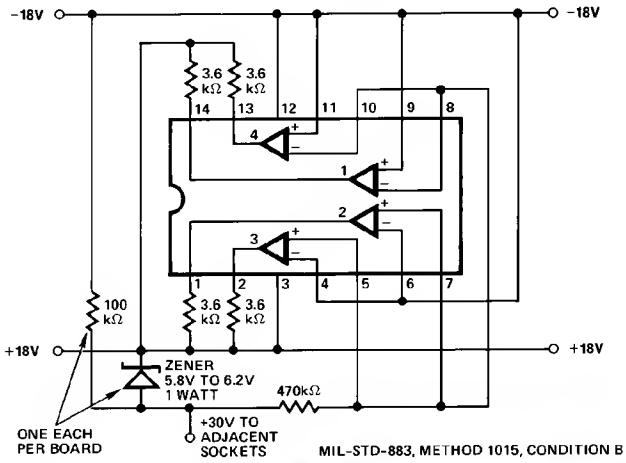
(@ V+ = +5 V, –55°C ≤ T_A ≤ +125°C for CMP04BY, –40°C ≤ T_A ≤ +85°C for CMP04FY/FP/FS, unless otherwise noted.)

Parameter	Symbol	Conditions	CMP04B/F[1] Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 0 Ω, R_L = 5.1 kΩ V_O = 1.4 V[2]		1 1	2 2	mV mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1 kΩ V_O = 1.4 V		4 4 4	20 20 20	nA nA nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		40	200	nA
Voltage Gain	A_V	R_L ≥ 15 kΩ, V+ = 15 V[3]	70	125		V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4 V[4] V_{RL} = 5 V, R_L = 5.1 kΩ		300 300 300		ns ns ns
Small-Signal Response Time	t_r	V_{IN} = 100 mV Step[4] 5 mV Overdrive V_{RL} = 5 V, R_L = 5.1 kΩ		1.3 1.3 1.3		µs µs µs
Input Voltage Range	CMVR	(Note 5)	0		V+–1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 1, 3)	60	100		dB
Power Supply Rejection Ratio	PSRR	V+ = +5 V to 18 V	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-)$ ≥ 1 V, $V_{IN}(+)$ = 0, I_{SINK} ≤ 4 mA		250 250	700 700	mV mV
Output Sink Current	I_{SINK}	$V_{IN}(-)$ ≥ 1 V, $V_{IN}(+)$ = 0, V_O ≤ 1.5 V	5 5	16 16		mA mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+)$ ≥ 1 V, $V_{IN}(-)$ = 0, V_O = 30 V		0.1 0.1	200 200	nA nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30 V		1.2 1.2	3.0 3.0	mA mA

NOTES
[1] R_L ≥ 15 kΩ, V+ = 15 V, V_{CM} = 1.5 V to 13.5 V.
[2] At output switch point, V_O = 1.4 V, R_S = 0 Ω with V+ from 5 V; and over the full input common-mode range (0 V to V+ –1.5 V).
[3] Guaranteed by design.
[4] Sample tested.
[5] The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+–1.5 V, but either or both inputs can go to +30 V without damage.

Specifications subject to change without notice.

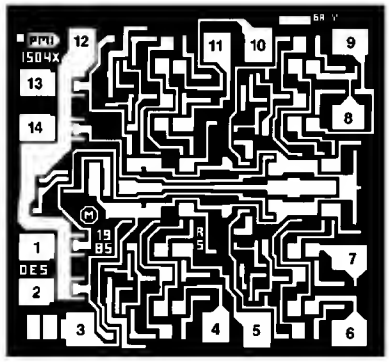
BURN-IN CIRCUIT



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DICE CHARACTERISTICS



1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NONINVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NONINVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NONINVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NONINVERTING INPUT (4)
12. GROUND (SUBSTRATE)
13. OUTPUT (4)
14. OUTPUT (3)

DIE SIZE 0.058 X 0.055 inch, 3190 sq. mils
(1.47 X 1.40 mm, 2.058 sq. mm)

WAFER TEST LIMITS (@ V+ = +5 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	CMP04N Limit	CMP04G Limit	Units
Input Offset Voltage	V_{OS}	$R_S = 0\ \Omega$, $R_L = 5.1\ k\Omega$ $V_O = 1.4\ V$[1]	1	2	mV max
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1\ k\Omega$ $V_O = 1.4\ V$	10	25	nA max
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$[1]	100	100	nA max
Voltage Gain	A_V	$R_L \geq 15\ k\Omega$, V+ = 15 V[3]	80	50	V/mV min
Input Voltage Range	CMVR	(Notes 2, 3)	V+–1.5	V+–1.5	V max
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB min
Power Supply Rejection Ratio	PSRR	V+ = 5 V to +18 V	80	80	dB min
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1\ V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4\ mA$	400	400	mV max
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1\ V$, $V_{IN}(+) = 0$, $V_O \leq 1.5\ V$	6	6	mA min
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1\ V$, $V_{IN}(-) = 0$, $V_O = 30\ V$	100	100	nA max
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30 V	2	2	mA max

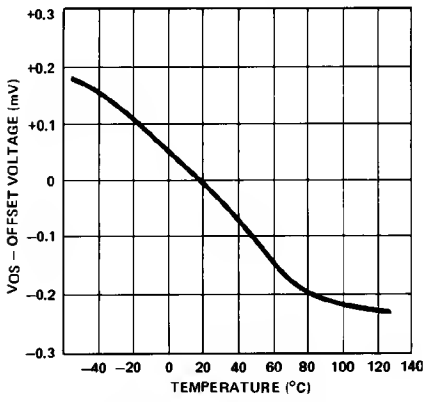
NOTES
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS (@ V+ = +5 V, unless otherwise noted.)

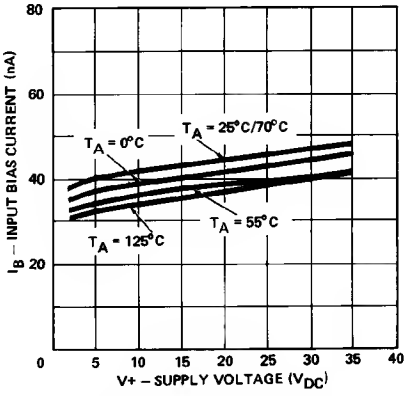
Parameter	Symbol	Conditions	CMP04N Typical	CMP04G Typical	Units
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4\ V$[5] $V_{RL} = 5\ V$, $R_L = 5.1\ k\Omega$	600	600	ns
Small-Signal Response Time	t_r	$V_{IN} = 100\ mV$ Step[5] 5 mV Overdrive $V_{RL} = 5\ V$, $R_L = 5.1\ k\Omega$	1.3	1.3	µs

NOTES
[1]At output switch point, $V_O = 1.4\ V$, $R_S = 0\ \Omega$ with V+ from 5 V; and over the full input common-mode range (0 V to V+ –1.5 V).
[2]The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to +30 V without damage.
[3]Guaranteed by design.
[4]$R_L \geq 15\ k\Omega$. V_{CM} = 1.5 V to 13.5 V.
[5]Sample tested.

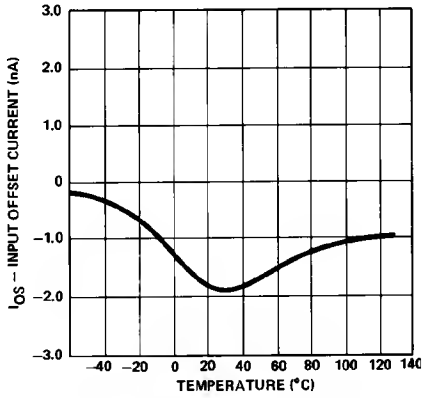
TYPICAL PERFORMANCE CHARACTERISTICS



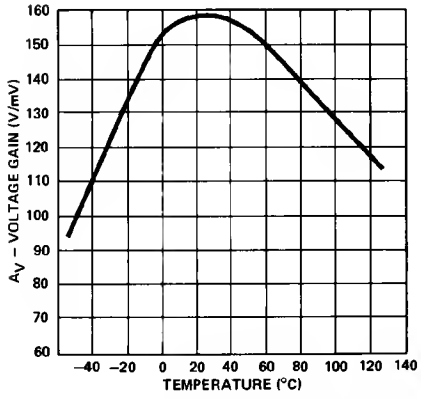
Offset Voltage vs. Temperature



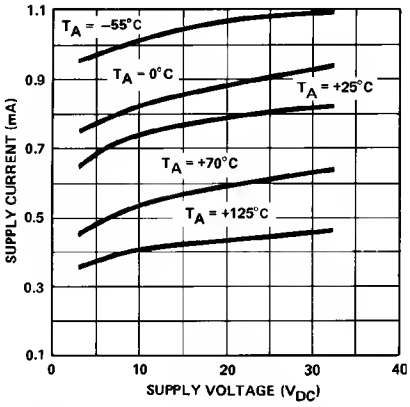
Input Bias Current vs. V+ and Temperature



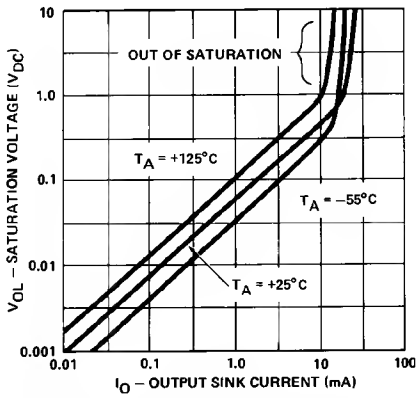
Input Offset Current vs. Temperature



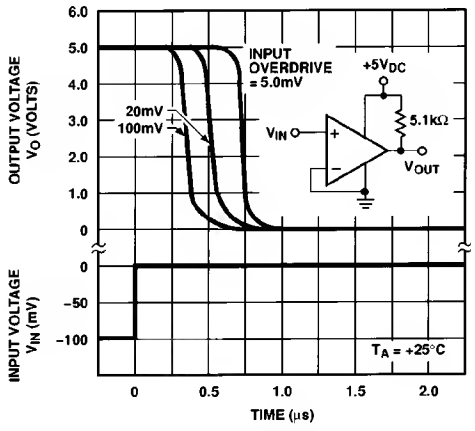
Voltage Gain vs. Temperature



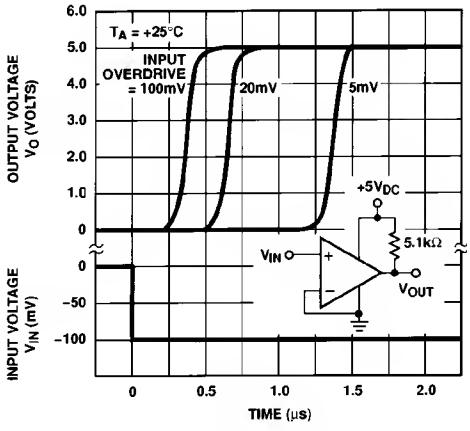
Supply Current vs. Supply Voltage



Output Voltage vs. Output Current and Temperature

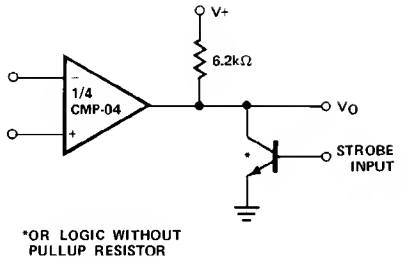


Response Time for Various Input Overdrives—Negative Transition

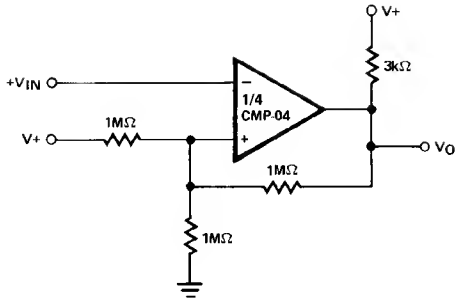


Response Time for Various Input Overdrives—Positive Transition

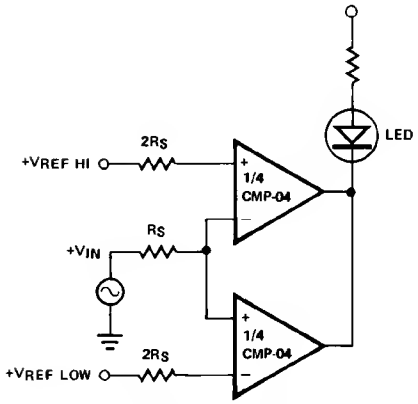
TYPICAL APPLICATIONS



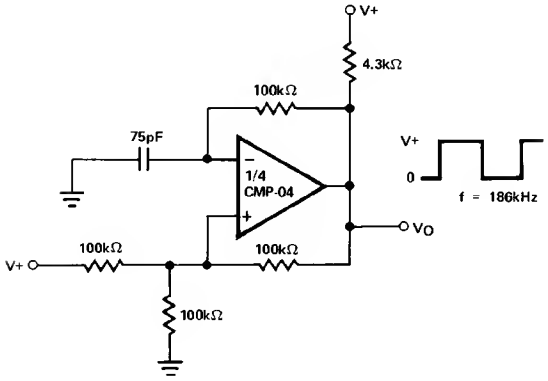
Output Strobing



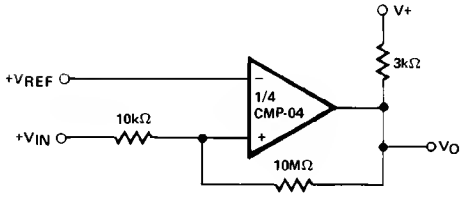
Inverting Comparator with Hysteresis



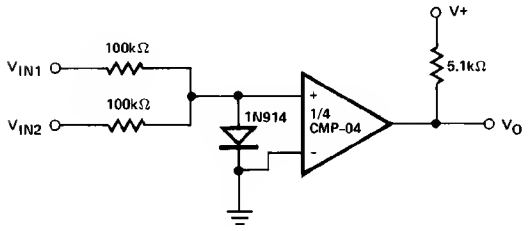
Limit Comparator



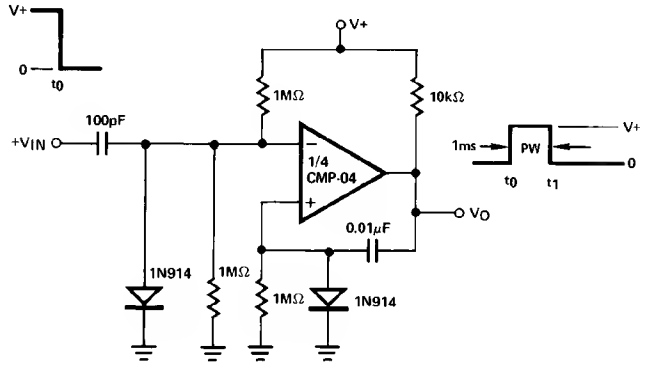
Squarewave Oscillator



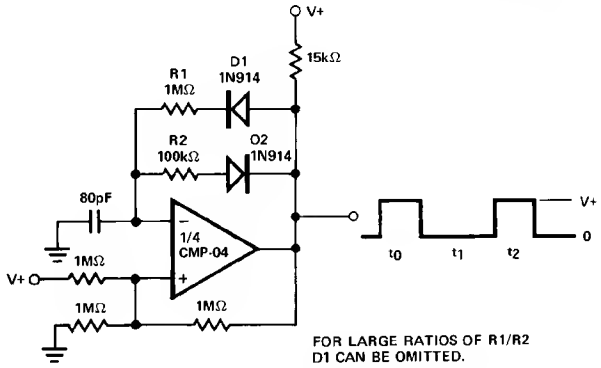
Noninverting Comparator with Hysteresis



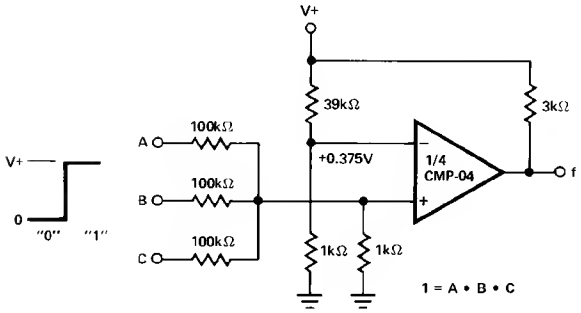
Comparing Input Voltages of Opposite Polarity



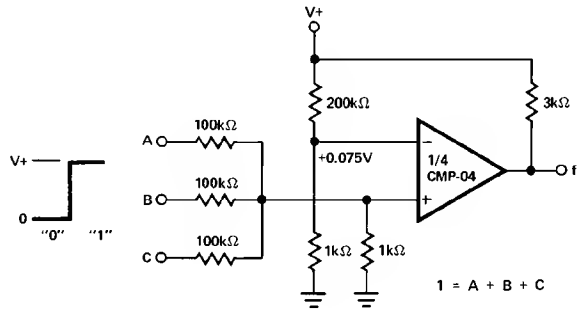
One-Shot Multivibrator



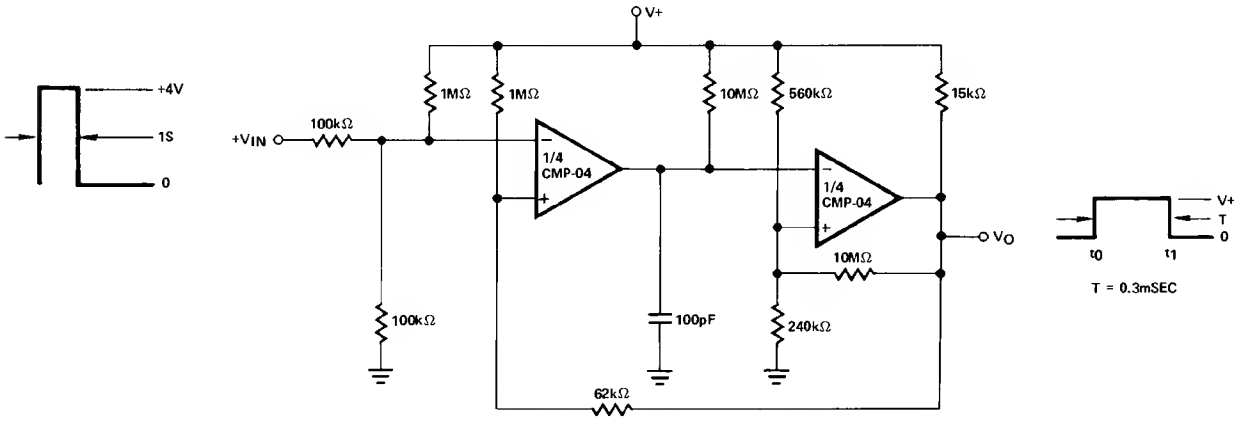
Pulse Generator



And Gate

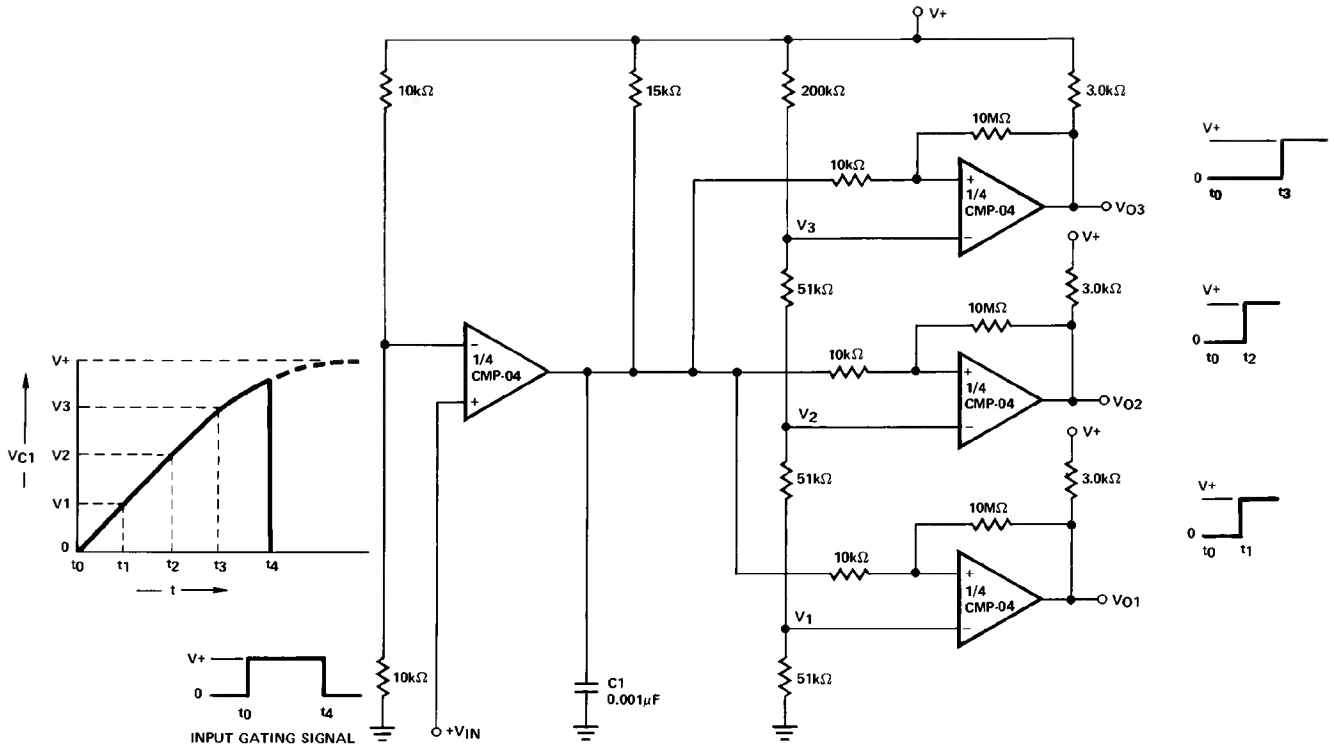


Or Gate



One-Shot Multivibrator with Input Lock Out

TYPICAL APPLICATIONS



Time Delay Generator